UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,804	06/27/2003	Seiichi Tomita	239565US2S	5899

22850 7590 11/04/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,804	TOMITA, SEIICHI	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-8* is/are allowed.

6)☒ Claim(s) *1,9 and 10* is/are rejected.

7)☒ Claim(s) *2-4 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information Disclosure Statement filed on 6-27-2003 is acknowledged by the examiner; A copy of a signed PTO-1449 attached with this office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Higashi (U.S. Patent 5,223,656).

Regarding claim 1:

Higashi discloses a semiconductor integrated circuit comprising: a first storage circuit configured to store a first value used to set a dead time (fig. 2, unit 1a); a second storage circuit configured to store a second value used to set a pulse width (fig. 2, unit 1b); an adder circuit configured to add the first value stored in the first storage circuit (fig. 2, unit 2a) and the second value stored in the second storage circuit (fig. 2, unit 2b), thereby outputting an addition result (fig. 3a, 3b); a timer configured to measure an elapsed time and output a count value indicative of the elapsed time (fig. 2, unit 1a, 1b); a first comparator circuit configured to compare the count value output from the timer with the addition result output

from the adder circuit (fig. 2, unit 2a, 3a, 4b); and a waveform-generating circuit configured to generate a pulse on the basis of a comparison result the first comparator circuit (fig. 2, unit 4a).

Regarding claim 9:

Higashi discloses a semiconductor integrated circuit comprising: a timer configured to measure an elapsed time and output a count value indicative of the elapsed time (fig. 2, unit 1a, 1b); a first storage circuit configured to store a first set value used to set a counting period of the timer (fig. 2, unit 1a); a second storage circuit configured to store a second set value used to set a pulse width of a first pulse (fig. 2, unit 1b); an operating circuit configured to compute a value indicative of the pulse width on the basis of the first set value stored in the first storage circuit and the second set value stored in the second storage circuit (fig. 2, unit 4a); a first comparator circuit configured to compare the count value output from the timer with the value indicative of the pulse width (fig. 2,, unit 2a, 2b) and computed by the operating circuit; and a first waveform-generating circuit configured to generate the first pulse on the basis of a comparison result of the first comparator circuit (fig. 2, unit 3a, 3b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill

in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi (U.S. Patent 5,223,656).

Higashi discloses the subject matter a device including the subject matter discussed above except the third storage circuit to store the value to set the dead time. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the working part, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8).

Claim Objections

4. Claims 2-4, 11, 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: regarding claim 2, prior art fail to teach the waveform generator define a leading edge of the pulse when the first comparator confirms the count value is identical to the addition result; Regarding claim 12, a second waveform circuit define the leading edge of the second pulse when the second comparator confirms that the count from timer is identical to the addition result; Regarding claim 11, a circuit to

define a trailing edge of the first pulse when the first comparator confirm the count value from the timer is identical to the value indicative of the pulse width.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 3, 4 are objected due to their dependency on claim 2.

Claims 13, 14 are objected due to their dependency on claim 12.

Allowable Subject Matter

5. Claims 5-8 are allowed.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

Independent claim 5 contains allowable subject matter. None of the prior art of record shows or fairly suggests the claimed invention.

Regarding claim 5:

The primary reason for the allowance of claim 5 is the inclusion of the semiconductor integrated circuit including a third storage circuit to store a leading

edge value to define a leading edge of the pulse. It is these features found in the claim, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes this claim allowable over the prior art.

Claims 6-8 are allowed due to their dependency on claim 5.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

John Barlow
Supervisory Patent Examiner
Technology Center 2800